Kindly replace claim 12 with the following amended claim 12:

12. (Three Times Amended) A method of manufacturing a semiconductor integrated circuit capacitor, comprising:

providing an insulating substrate;

simultaneously forming a first wire line and a lower electrode on predetermined surfaces of the insulating surfaces;

forming an interlevel insulating layer on the substrate, on the first wire line, and on the lower electrode;

selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole having sidewalls and disposed above the lower electrode; and (ii) a second via hole disposed above the first wire line;

forming a tungsten containing conductive layer on the interlevel insulating layer and in the first and second via holes;

performing a tungsten etch back process to selectively etch back the tungsten containing conductive layer on the interlevel insulating layer and in the first and second via holes to simultaneously form: (i) a tungsten containing conductive sidewall spacer from the tungsten containing conductive layer formed in the first via hole and on the sidewalls of the first via hole for preventing dielectric disconnection; (ii) a tungsten containing conductive plug from the tungsten containing conductive layer formed in the second via hole, the tungsten containing conductive sidewall spacer and the tungsten containing conductive plug being formed of the same tungsten containing conductive layer; and (iii) an exposed surface containing the spacer, conductive plug, the

predetermined surface of the lower electrode, and predetermined surfaces of the interlevel insulating layer;

forming a dielectric layer on the exposed surface, the tungsten containing conductive sidewall spacer and the tungsten containing conductive layer formed in the first via hole;

removing the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on the tungsten containing conductive sidewall spacer and predetermined surface of the lower electrode; and

simultaneously forming: (i) a second wire line connected to the tungsten containing conductive plug; and (ii) an upper electrode connected to the dielectric layer.

The changes in the previous paragraph are indicated by brackets for deletions and underlining for insertions.

12. (Three Times Amended) A method of manufacturing a semiconductor integrated circuit capacitor, comprising:

providing an insulating substrate;

simultaneously forming a first wire line and a lower electrode on predetermined surfaces of the insulating surfaces;

forming an interlevel insulating layer on the substrate, on the first wire line, and on the lower electrode;

selectively etching the interlevel insulating layer to expose a predetermined surface of the lower electrode and a predetermined surface of the first wire line thereby simultaneously forming in the interlevel insulating layer: (i) a first via hole having sidewalls and disposed above the lower electrode; and (ii) a second via hole disposed above the first wire line;

forming a tungsten containing conductive layer on the interlevel insulating layer and in the first and second via holes;

performing a tungsten etch back process to selectively etch back the tungsten containing conductive layer on the interlevel insulating layer and in the first and second via holes to simultaneously form: (i) a tungsten containing conductive sidewall spacer [on] from the tungsten containing conductive layer formed in the first via hole and on the sidewalls of the first via hole for preventing dielectric disconnection; (ii) a tungsten containing conductive plug from the tungsten containing conductive layer formed in the second via hole, the tungsten containing conductive sidewall spacer and the tungsten containing conductive plug being formed of the same tungsten

containing conductive layer; and (iii) an exposed surface containing the spacer, conductive plug, the predetermined surface of the lower electrode, and predetermined surfaces of the interlevel insulating layer;

forming a dielectric layer on the exposed surface, the tungsten containing conductive sidewall spacer and the tungsten containing conductive layer formed in the first via hole;

removing the dielectric layer on the exposed surface except for a predetermined portion of the dielectric layer disposed on the tungsten containing conductive sidewall spacer and predetermined surface of the lower electrode; and

simultaneously forming: (i) a second wire line connected to the tungsten containing conductive plug; and (ii) an upper electrode connected to the dielectric layer.